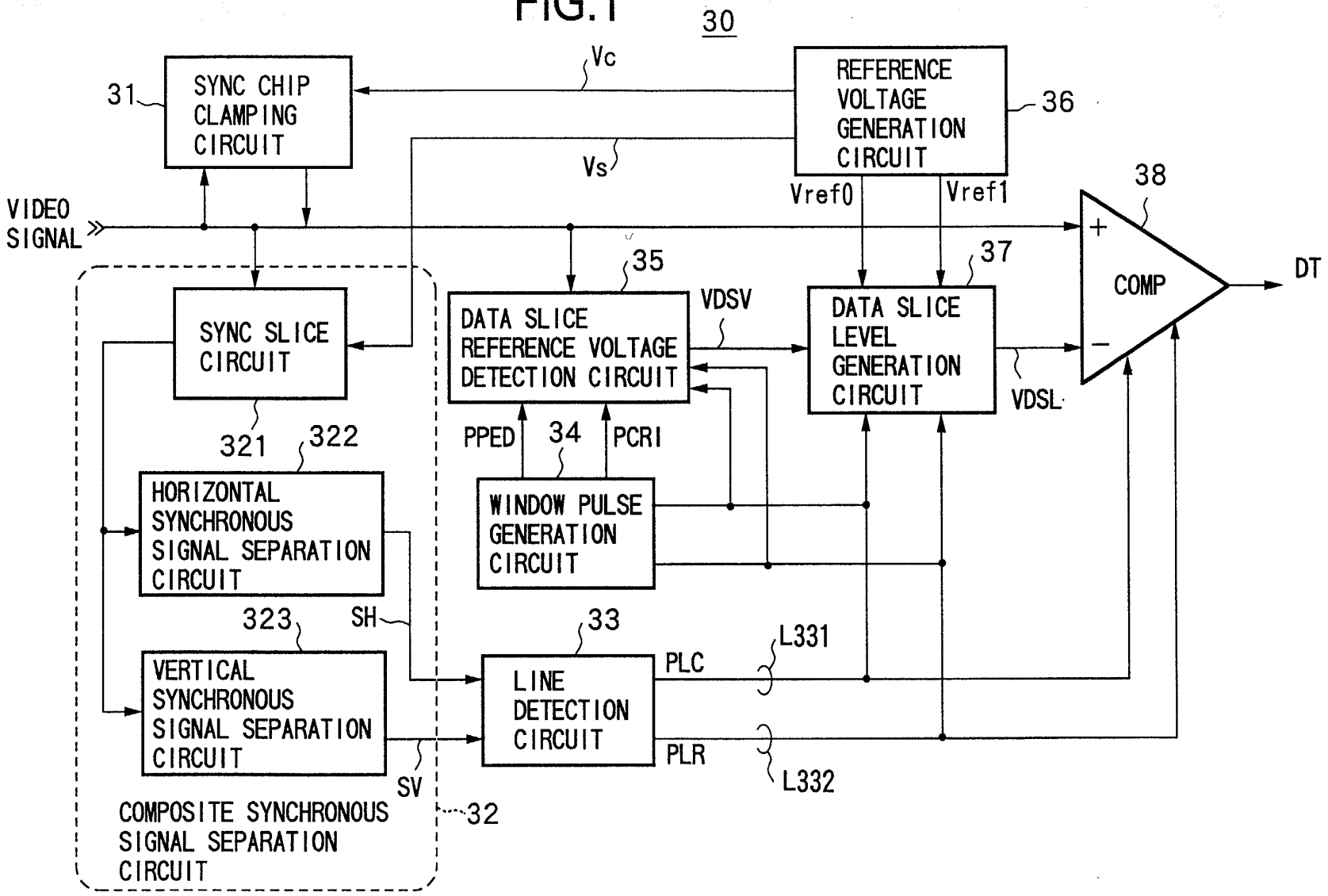
FIG.1


30
31
SYNC CHIP CLAMPING CIRCUIT
Vc
Vs
REFERENCE VOLTAGE GENERATION CIRCUIT
36
Vref0
Vref1
38
VIDEO SIGNAL
35
37
COMP
DT
SYNC SLICE CIRCUIT
DATA SLICE REFERENCE VOLTAGE DETECTION CIRCUIT
VDSV
DATA SLICE LEVEL GENERATION CIRCUIT
VDSL
321
322
PPED
34
PCRI
HORIZONTAL SYNCHRONOUS SIGNAL SEPARATION CIRCUIT
WINDOW PULSE GENERATION CIRCUIT
323
SH
33
L331
VERTICAL SYNCHRONOUS SIGNAL SEPARATION CIRCUIT
LINE DETECTION CIRCUIT
PLC
PLR
L332
SV
COMPOSITE SYNCHRONOUS SIGNAL SEPARATION CIRCUIT
32

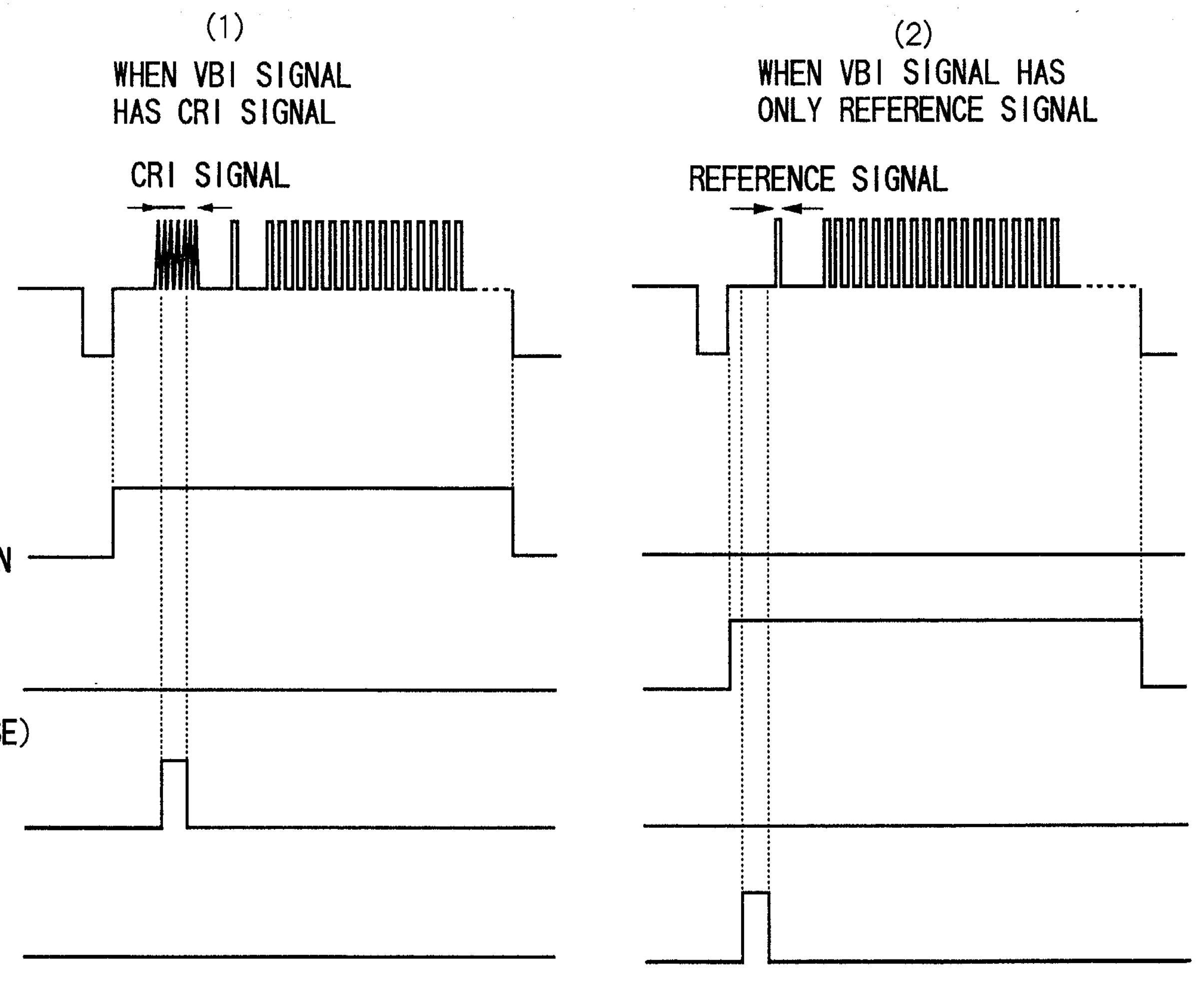


FIG.2A VBI (VIDEO SIGNAL)

FIG.2B PLC (LINE DETECTION PULSE)

FIG.2C PLR (LINE DETECTION PULSE)

FIG.2D PCRI (WINDOW PULSE)

FIG.2E PPED (WINDOW PULSE)

FIG.3

35A

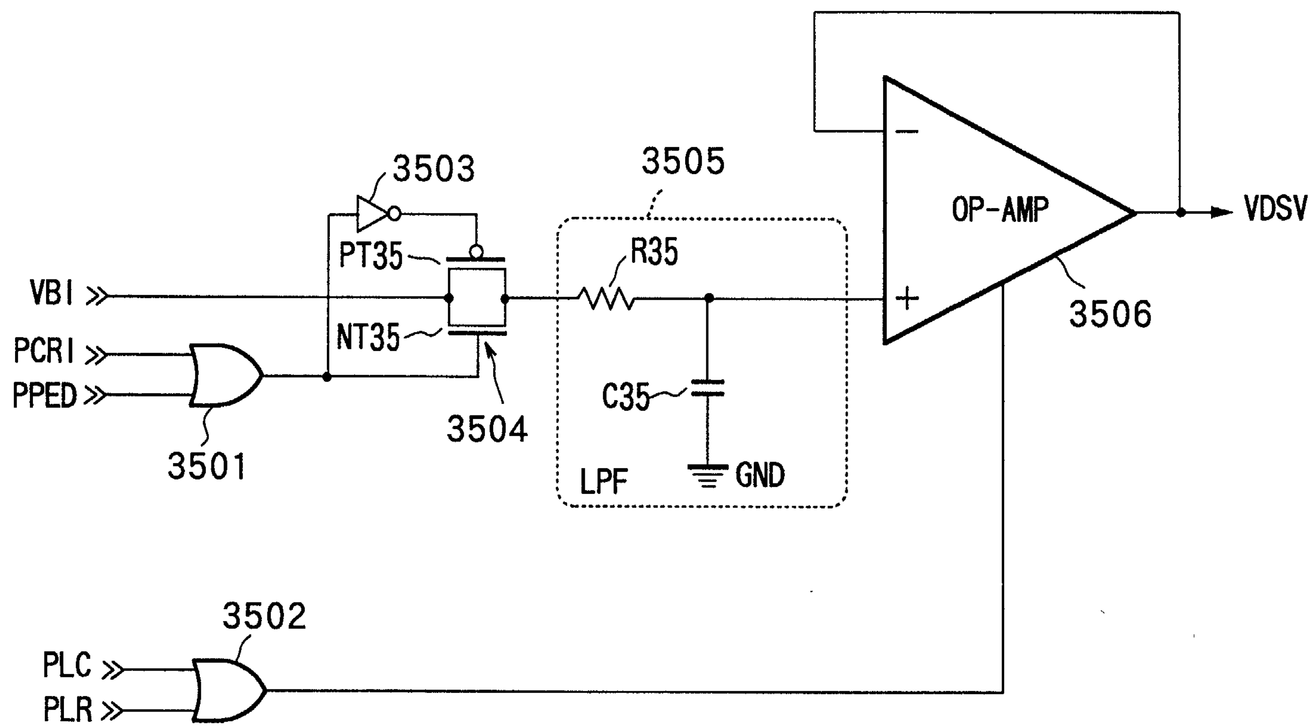

3503
3505
PT35
R35
VBI
NT35
PCRI
PPED
3504
3501
C35
GND
LPF
OP-AMP
VDSV
3506
3502
PLC
PLR

FIG.4

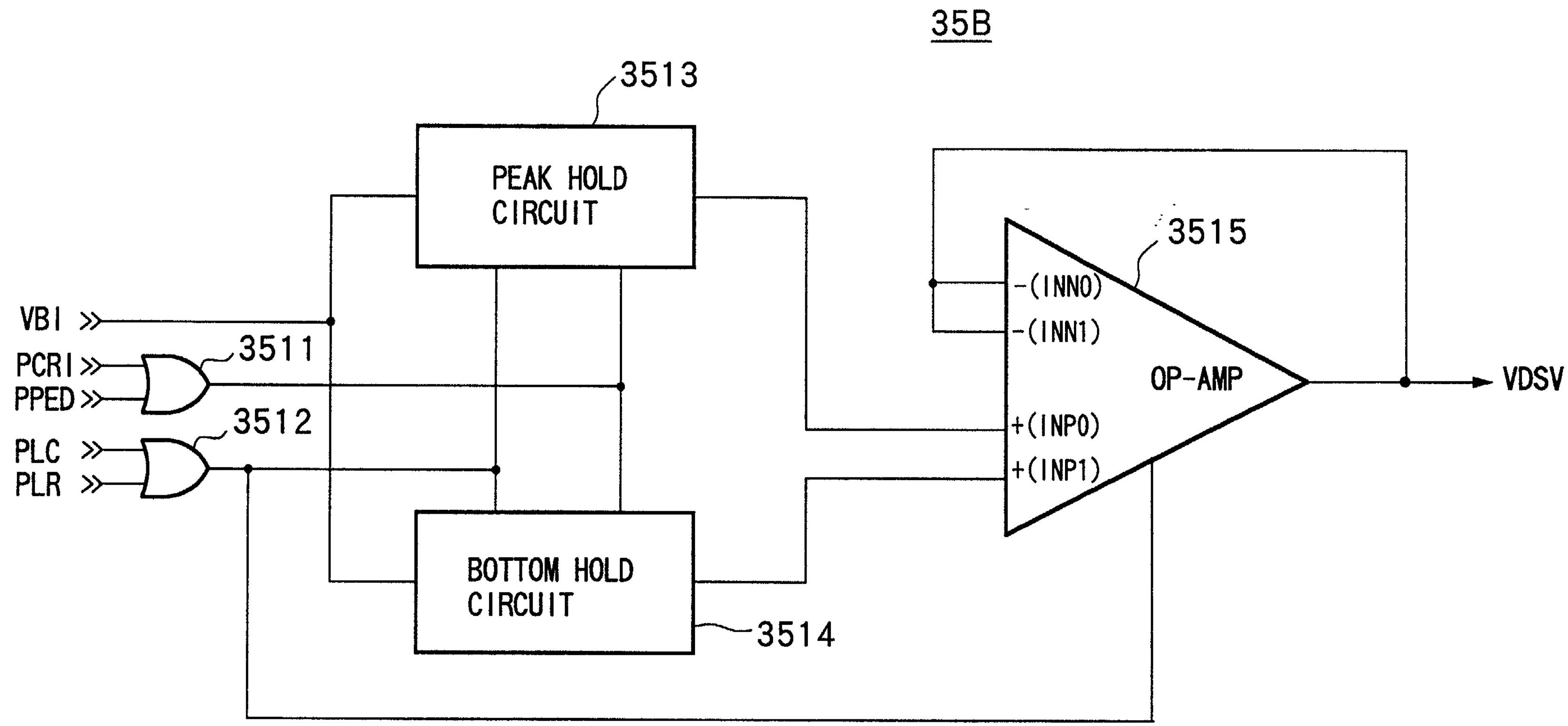
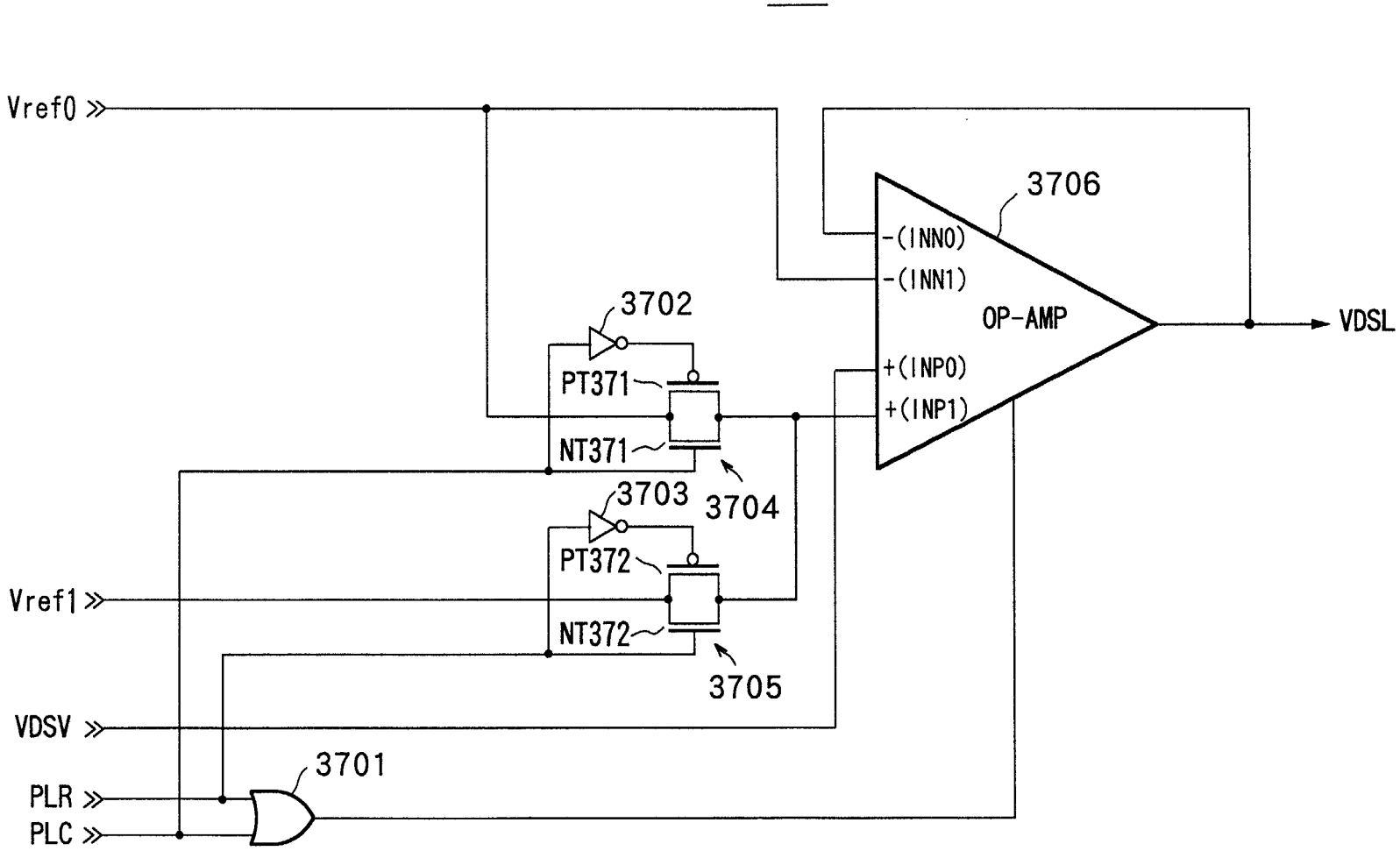

35B
3513
PEAK HOLD CIRCUIT
3514
BOTTOM HOLD CIRCUIT
3515
OP-AMP
-(INN0)
-(INN1)
+(INP0)
+(INP1)
VDSV
3511
3512
VBI
PCRI
PPED
PLC
PLR

FIG.5


37A
Vref0
3706
-(INN0)
-(INN1)
OP-AMP
VDSL
+(INP0)
+(INP1)
3702
PT371
NT371
3704
3703
PT372
Vref1
NT372
3705
VDSV
3701
PLR
PLC

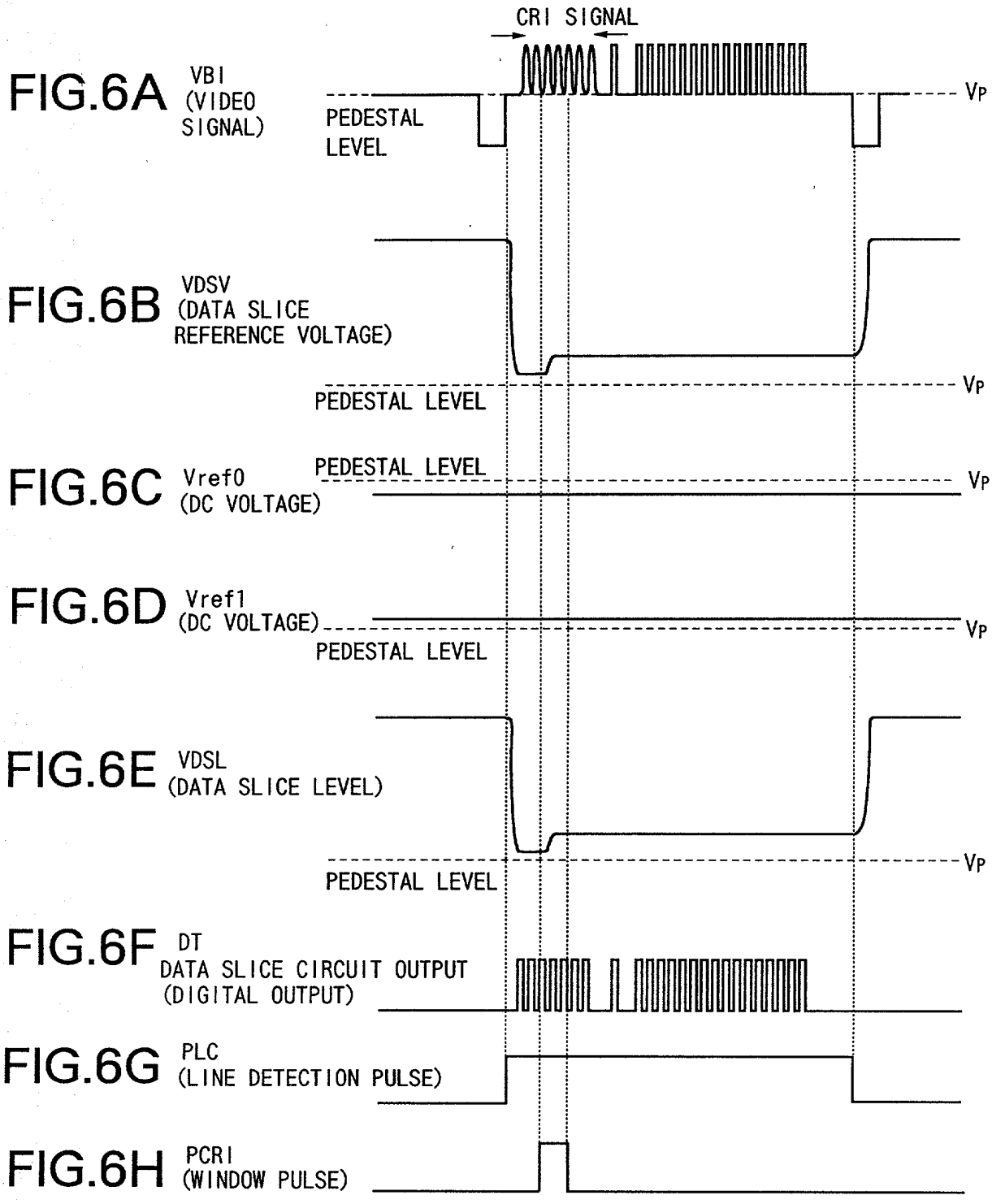

CRI SIGNAL
FIG.6A VBI (VIDEO SIGNAL)
PEDESTAL LEVEL
VP
FIG.6B VDSV (DATA SLICE REFERENCE VOLTAGE)
PEDESTAL LEVEL
VP
FIG.6C Vref0 (DC VOLTAGE)
PEDESTAL LEVEL
VP
FIG.6D Vref1 (DC VOLTAGE)
PEDESTAL LEVEL
VP
FIG.6E VDSL (DATA SLICE LEVEL)
PEDESTAL LEVEL
VP
FIG.6F DT
DATA SLICE CIRCUIT OUTPUT
(DIGITAL OUTPUT)
FIG.6G PLC
(LINE DETECTION PULSE)
FIG.6H PCRI
(WINDOW PULSE)

FIG.7A
FIG.7B
FIG.7C
FIG.7D
FIG.7E
FIG.7F
FIG.7G
FIG.7H

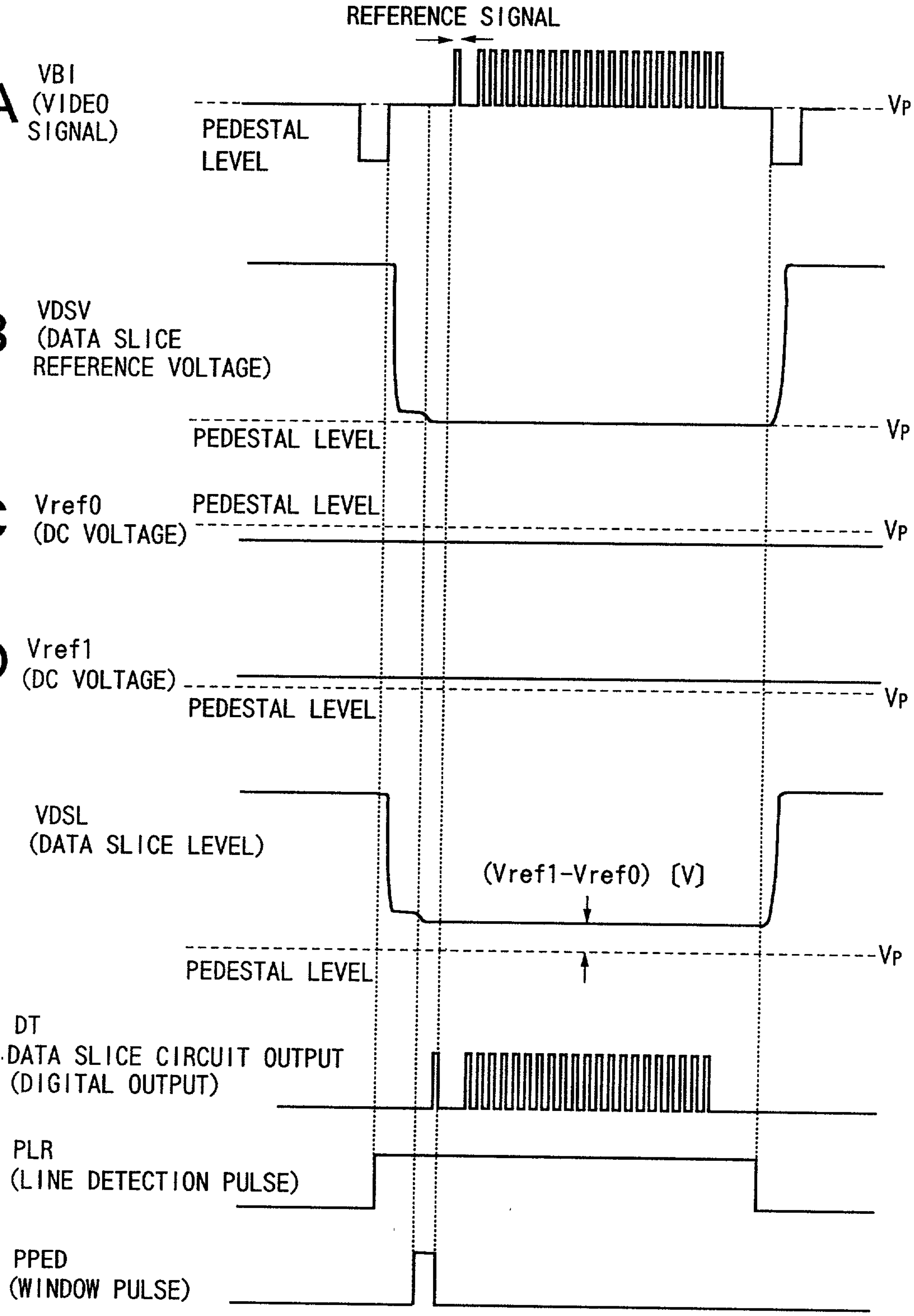


FIG.8

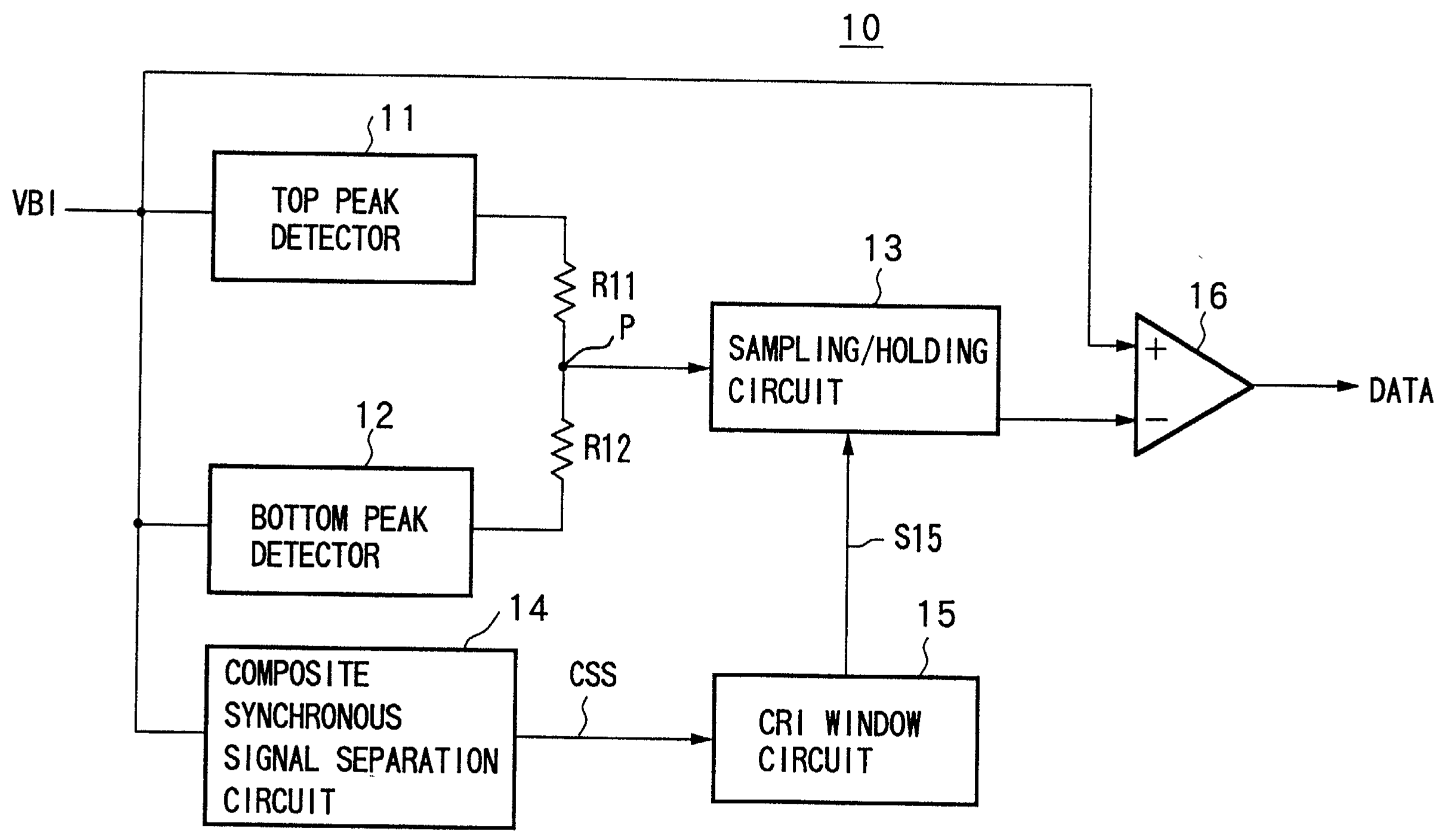
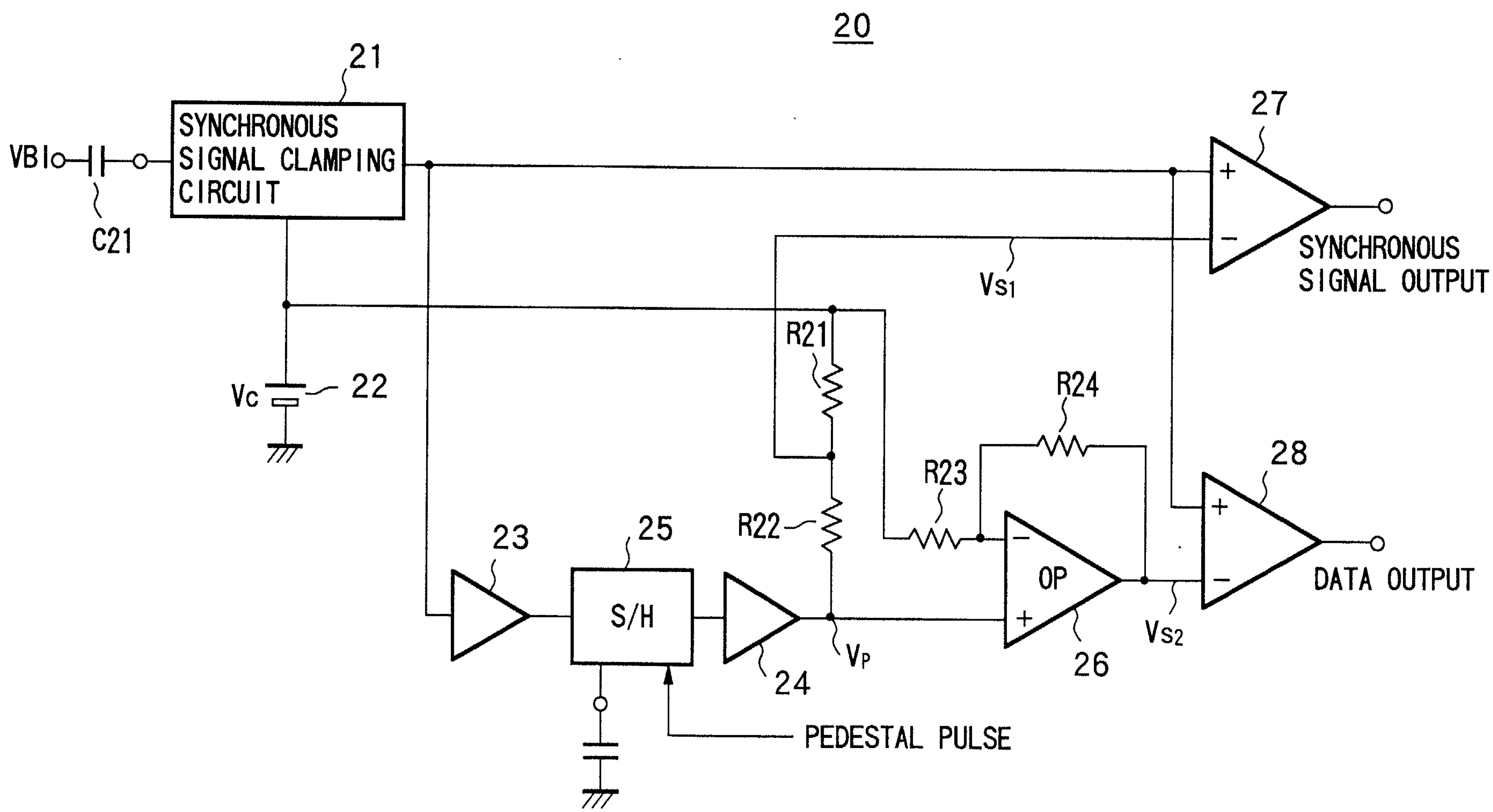

10
VBI
11
TOP PEAK DETECTOR
12
BOTTOM PEAK DETECTOR
14
COMPOSITE SYNCHRONOUS SIGNAL SEPARATION CIRCUIT
R11
P
R12
CSS
13
SAMPLING/HOLDING CIRCUIT
S15
15
CRI WINDOW CIRCUIT
16
+
−
DATA

FIG.9


20
21
SYNCHRONOUS SIGNAL CLAMPING CIRCUIT
VBI
C21
Vc
22
23
25
S/H
24
PEDESTAL PULSE
R21
R22
R23
R24
Vp
OP
26
Vs1
Vs2
27
28
SYNCHRONOUS SIGNAL OUTPUT
DATA OUTPUT